ADCCONV PAGE 1

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3 ; Author : ADI - Apps

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5 ; Date : 5 November 2001

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7 ; File : adcconv.asm

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9 ; Hardware : ADuC836

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11 ; Description : example routine to continuosuly trigger

12 ; a single conversion on the ADC main channel

13 ; The Conversion result is written to external memory,

14 ; P3.4 is toggled 5 times at 100ms delay

15 ; The ADC result is written to external memory

16 ; P3.4 is toggled 5 times at 500ms

17 ; and the sequence repeats itself.

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19 ;======================================================================

20 ;

21 $MOD836 ; Use 8052&ADuC836 predefined symbols

22

0000 23 FLAG EQU 00H ; Define Bit

24

25

---- 26 CSEG ; Defines the following as a segment of code

27

0000 28 ORG 0000H ; Load Code at '0'

29

0000 020060 30 JMP START ; Jump to START

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32 ;======================================================================

33 ;

0033 34 ORG 0033H ; Read ADC Result H/M/L to external Memory

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36 ; 10 flashes at 100ms

0033 7401 37 MOV A,#01H ; 100msec delay

0035 7B0A 38 MOV R3,#0Ah ; loop=5

0037 B2B4 39 TIC1: CPL P3.4 ; Toggle LED

0039 120079 40 CALL DELAY ; Delay 100mSec

003C DBF9 41 DJNZ R3,TIC1 ; Dec loop

42

003E 900000 43 MOV DPTR, #00H ; DPTR=00

0041 E5DA 44 MOV A,ADC0M ; read ADC Middle byte

0043 F0 45 MOVX @DPTR,A ; write Middle byte to ext memory

0044 A3 46 INC DPTR ; DPTR=01

0045 E5DB 47 MOV A,ADC0H ; read ADC High byte

0047 F0 48 MOVX @DPTR,A ; write low High byte to ext memory

0048 A3 49 INC DPTR

50

51 ; 5 flashes at 500ms

0049 7405 52 MOV A,#05H ; 500msec delay

004B 7B0A 53 MOV R3,#0Ah ; loop=10

004D B2B4 54 TIC2: CPL P3.4 ; Toggle LED

004F 120079 55 CALL Delay ; Delay 100mSec

0052 DBF9 56 DJNZ R3,TIC2 ; Dec loop

57 ;

0054 D200 58 SETB Flag ; Set Flag

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59

0056 32 60 RETI ; Return from Interrupt

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62 ;======================================================================

63 ;

0060 64 ORG 0060H

0060 65 START:

66 ; Configure Interrupt System

0060 D288 67 SETB IT0 ; CONFIG EXTERNAL INTERRUPT Falling Edge

0062 D2AF 68 SETB EA ; Enable Global Interrupts

69

70 ; Configure ADC

0064 75D120 71 MOV ADCMODE,#20H ; ENABLE MAIN ADC; Mode- Power down

0067 75D240 72 MOV ADC0CON,#40H ; 24 BITS

73 ; USE EXTERNAL REFERENCE

74 ; AIN1-AIN2

75 ; BIPOLAR MODE

76 ; RANGE = +/-20mV

006A D2AE 77 SETB EADC ; ENABLE ADC INTERRUPT

78

79 ; Looped single conversions

006C C200 80 CONV: CLR FLAG ; Initial condition for FLAG variable

006E 75D122 81 MOV ADCMODE,#22H ; INITIATE A MAIN ADC SINGLE CONVERSION

0071 120079 82 CALL DELAY ; Jump to subroutine DELAY

0074 3000FD 83 JNB FLAG,$ ; Stay here until FLAG=1 i.e. wait for ADC Int.

0077 80F3 84 JMP CONV ; Next ADC Conversion

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87 ;

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0079 89 DELAY: ; Delays by A\*100ms (default Core Clk =1.57MHz)

0079 F8 90 MOV R0,A ; Acc holds delay variable

007A 79FE 91 DLY0: MOV R1,#0FEh ; Set up delay loop0

007C 7A19 92 DLY1: MOV R2,#019h ; Set up delay loop1

007E DAFE 93 DJNZ R2,$ ; Dec R2 & Jump here until R2 is 0

0080 D9FA 94 DJNZ R1,DLY1 ; Dec R1 & Jump DLY1 until R1 is 0

0082 D8F6 95 DJNZ R0,DLY0 ; Dec R0 & Jump DLY0 until R0 is 0

0084 22 96 RET ; Return from subroutine

97 ;

98 END

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100

101

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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ADC0CON. . . . . . . . . . . . . D ADDR 00D2H PREDEFINED

ADC0H. . . . . . . . . . . . . . D ADDR 00DBH PREDEFINED

ADC0M. . . . . . . . . . . . . . D ADDR 00DAH PREDEFINED

ADCMODE. . . . . . . . . . . . . D ADDR 00D1H PREDEFINED

CONV . . . . . . . . . . . . . . C ADDR 006CH

DELAY. . . . . . . . . . . . . . C ADDR 0079H

DLY0 . . . . . . . . . . . . . . C ADDR 007AH

DLY1 . . . . . . . . . . . . . . C ADDR 007CH

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EADC . . . . . . . . . . . . . . B ADDR 00AEH PREDEFINED

FLAG . . . . . . . . . . . . . . NUMB 0000H

IT0. . . . . . . . . . . . . . . B ADDR 0088H PREDEFINED

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

START. . . . . . . . . . . . . . C ADDR 0060H

TIC1 . . . . . . . . . . . . . . C ADDR 0037H

TIC2 . . . . . . . . . . . . . . C ADDR 004DH